

1



Date: Monday, January 14, 2008 Sheet 1 of 45

ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M IDE Integrated Series
Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
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PCI Routing

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

ICH8M Integrated Pull-up
and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

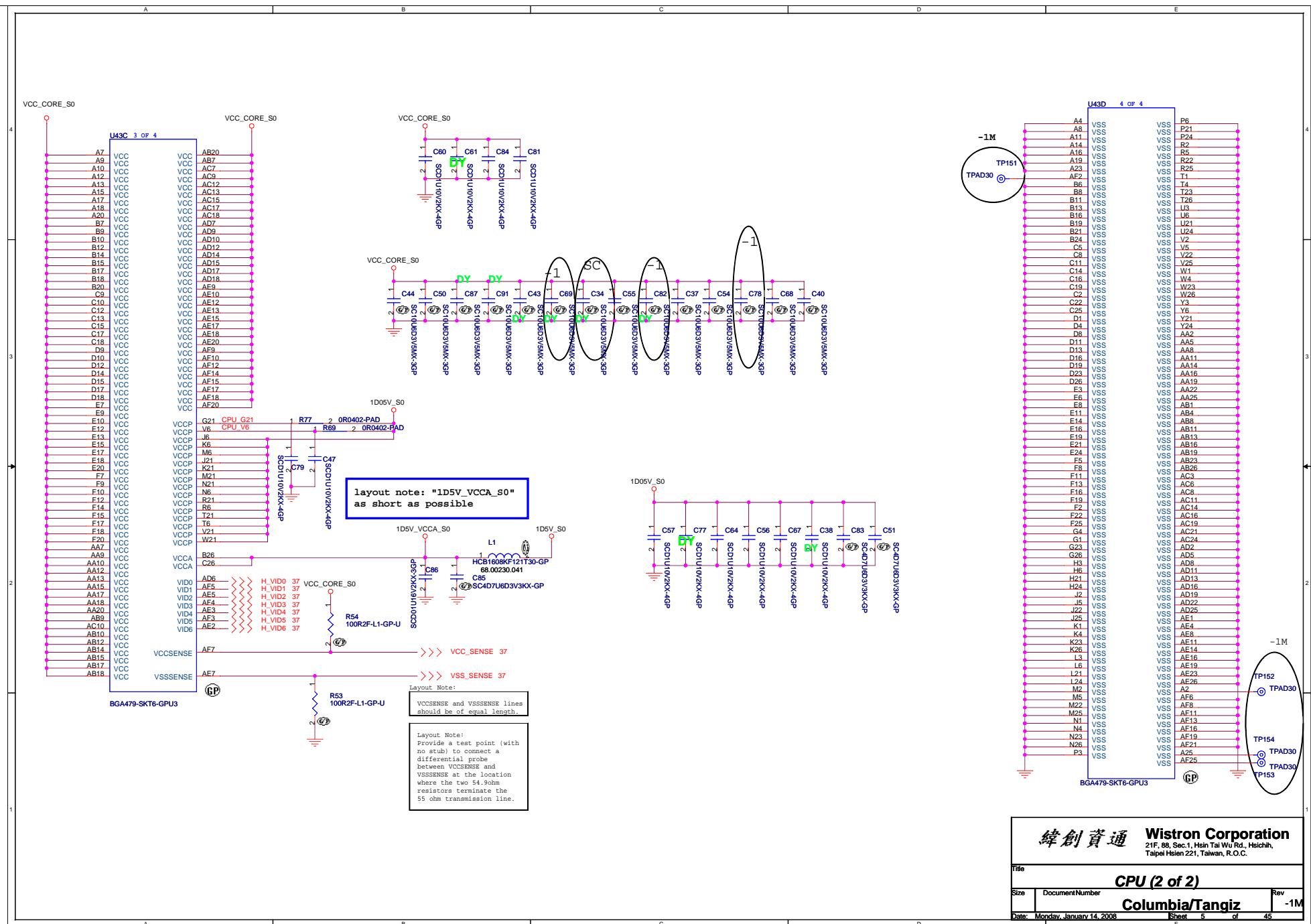
Crestline Strapping Signals and
Configuration

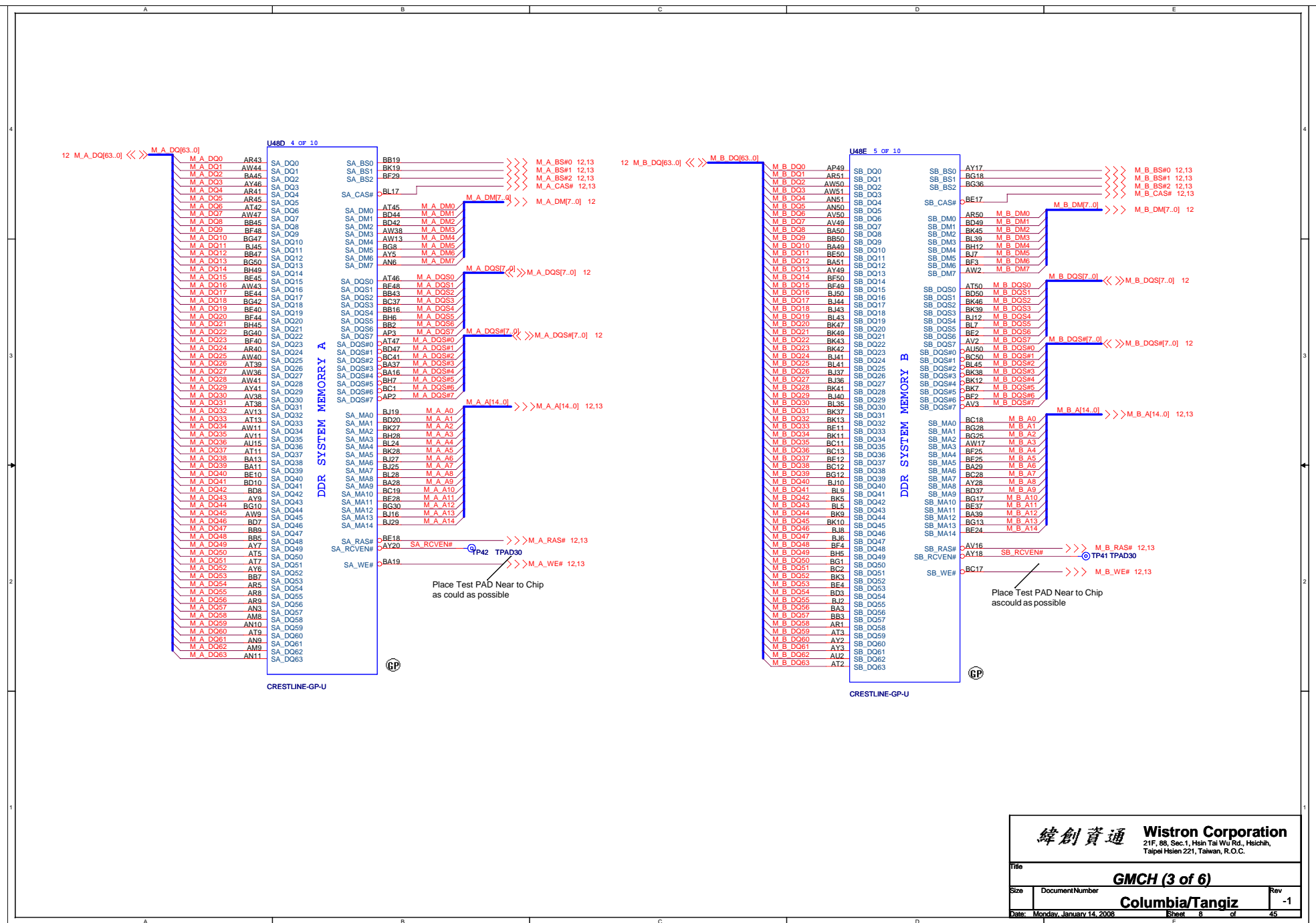
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE xl is operational (Default) 1 =SDVO and PCIE xl are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading
edge of the Crestline GMCH PWROK in signal.

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipai Hsien 221, Taiwan, R.O.C.	
Title	
Reference	
Size A3	Document Number Columbia/Tangiz
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Rev -1M	

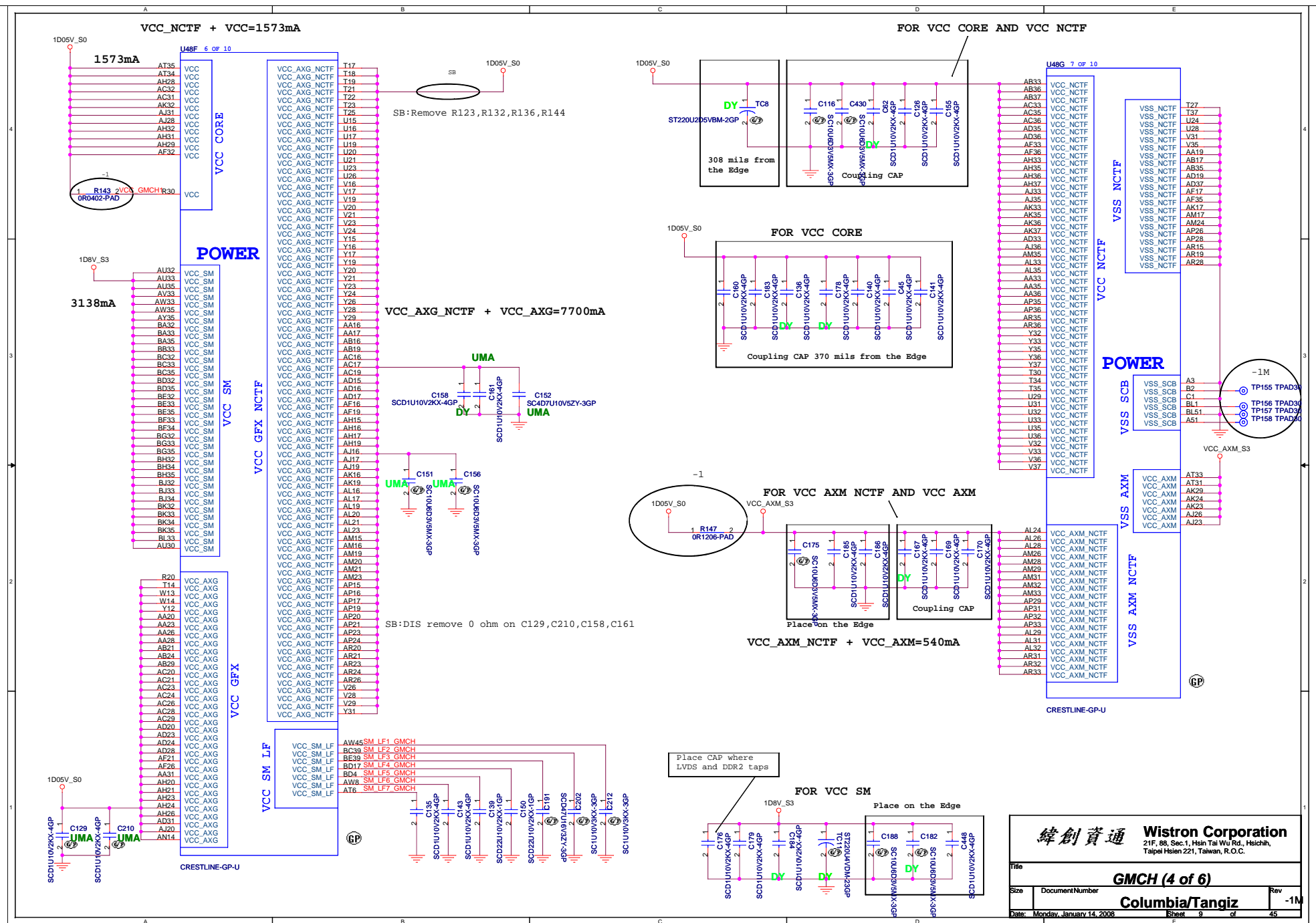


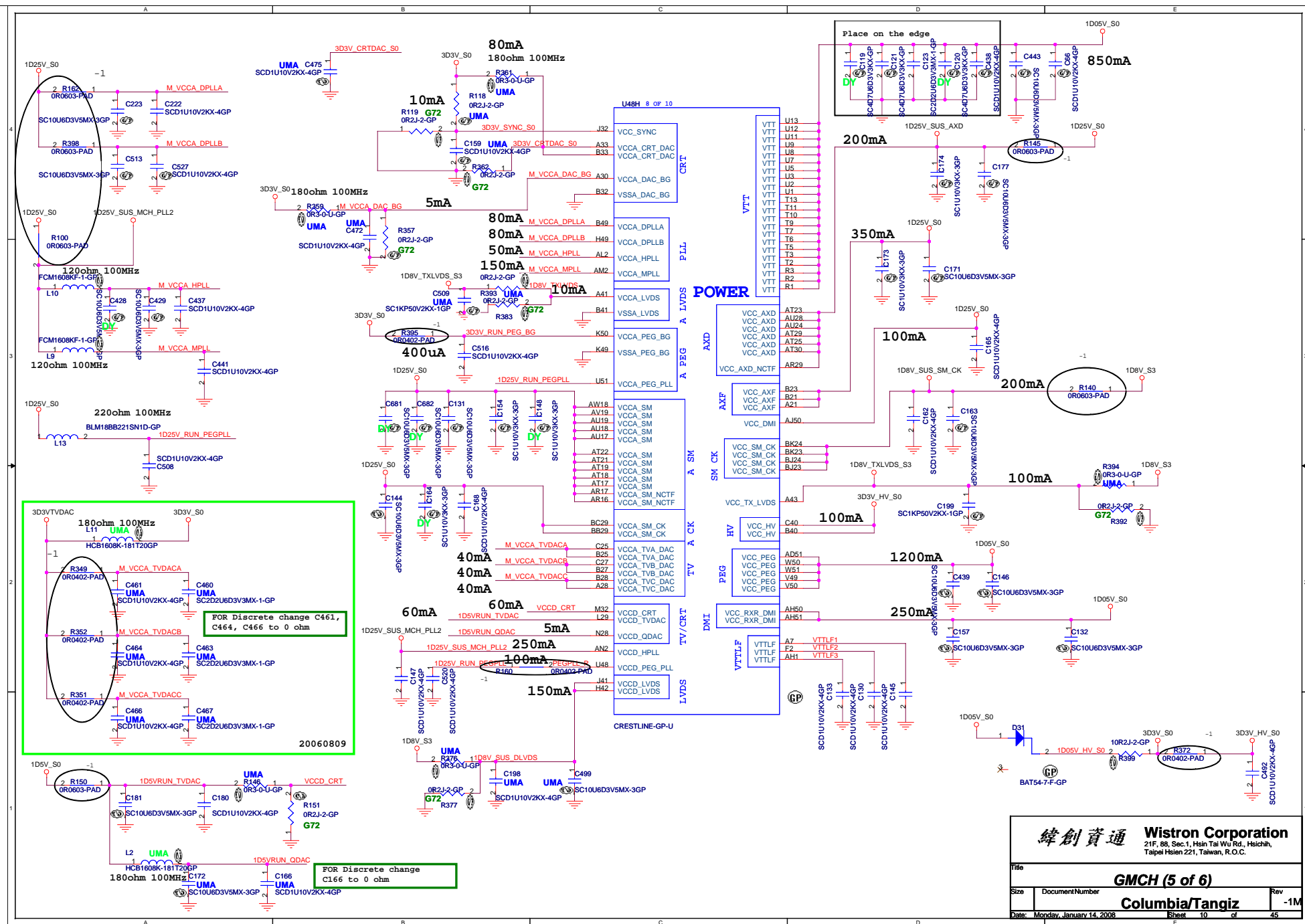


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Columbia/Tangiz





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A13	VSS	VSS	AW24
A15	VSS	VSS	AW29
A17	VSS	VSS	AW32
A24	VSS	VSS	AW5
AA21	VSS	VSS	AW7
AA24	VSS	VSS	AY10
AA29	VSS	VSS	AY24
AB20	VSS	VSS	AY37
AB23	VSS	VSS	AY42
AB26	VSS	VSS	AY43
AB28	VSS	VSS	AY45
AB31	VSS	VSS	AY47
AC10	VSS	VSS	AY50
AC13	VSS	VSS	B10
AC3	VSS	VSS	B20
AC39	VSS	VSS	B24
AC43	VSS	VSS	B29
AC47	VSS	VSS	B30
AD1	VSS	VSS	B35
AD21	VSS	VSS	B38
AD26	VSS	VSS	B43
AD28	VSS	VSS	B46
AD3	VSS	VSS	B5
AD41	VSS	VSS	B8
AD45	VSS	VSS	BA1
AD48	VSS	VSS	BA17
AD5	VSS	VSS	BA18
AD50	VSS	VSS	BA2
AD8	VSS	VSS	BA24
AE10	VSS	VSS	BB12
AE14	VSS	VSS	BB25
AE6	VSS	VSS	BB40
AF20	VSS	VSS	BB44
AF23	VSS	VSS	BB49
AF24	VSS	VSS	BB8
AF31	VSS	VSS	BC16
AG2	VSS	VSS	BC24
AG38	VSS	VSS	BC25
AG43	VSS	VSS	BC36
AG47	VSS	VSS	BC40
AG50	VSS	VSS	BC51
AH3	VSS	VSS	BD13
AH40	VSS	VSS	BD2
AH41	VSS	VSS	BD28
AH7	VSS	VSS	BD45
AH9	VSS	VSS	BD48
AJ11	VSS	VSS	BD5
AJ13	VSS	VSS	BE1
AJ21	VSS	VSS	BE19
AJ24	VSS	VSS	BE23
AJ29	VSS	VSS	BE30
AJ32	VSS	VSS	BE42
AJ43	VSS	VSS	BE51
AJ45	VSS	VSS	BE8
AJ49	VSS	VSS	BF12
AK20	VSS	VSS	BF16
AK21	VSS	VSS	BF36
AK26	VSS	VSS	BG19
AK28	VSS	VSS	BG2
AK31	VSS	VSS	BG24
AK51	VSS	VSS	BG29
AL1	VSS	VSS	BG39
AM11	VSS	VSS	BG48
AM13	VSS	VSS	BG5
AM3	VSS	VSS	BG51
AM4	VSS	VSS	BH17
AM41	VSS	VSS	BH30
AM45	VSS	VSS	BH44
AN1	VSS	VSS	BH46
AN38	VSS	VSS	BH8
AN39	VSS	VSS	BJ11
AN43	VSS	VSS	BJ13
AN5	VSS	VSS	BJ38
AN7	VSS	VSS	BJ4
AP4	VSS	VSS	BJ42
AP48	VSS	VSS	BJ46
AP50	VSS	VSS	BK15
AR11	VSS	VSS	BK17
AR2	VSS	VSS	BK25
AR38	VSS	VSS	BK29
AR44	VSS	VSS	BK36
AR47	VSS	VSS	BK40
AR7	VSS	VSS	BK44
AT10	VSS	VSS	BK6
AT14	VSS	VSS	BK8
AT41	VSS	VSS	BL11
AT49	VSS	VSS	BL13
AU1	VSS	VSS	BL19
AU23	VSS	VSS	BL22
AU29	VSS	VSS	BL37
AU3	VSS	VSS	BL47
AU36	VSS	VSS	C12
AU49	VSS	VSS	C16
AU51	VSS	VSS	C19
AV39	VSS	VSS	C28
AV48	VSS	VSS	C29
AW1	VSS	VSS	C33
AW12	VSS	VSS	C36
AW16	VSS	VSS	C41

VSS

CRESTLINE-GP-U

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C46	VSS	VSS	W11
C50	VSS	VSS	W39
C7	VSS	VSS	W43
D13	VSS	VSS	W47
D24	VSS	VSS	W5
D3	VSS	VSS	W7
D32	VSS	VSS	Y13
D39	VSS	VSS	Y2
D45	VSS	VSS	Y41
D49	VSS	VSS	Y45
E10	VSS	VSS	Y49
E16	VSS	VSS	Y5
E24	VSS	VSS	Y50
E29	VSS	VSS	Y11
E32	VSS	VSS	P29
E47	VSS	VSS	T29
F19	VSS	VSS	T31
F36	VSS	VSS	T33
F4	VSS	VSS	R28
F40	VSS	VSS	
F50	VSS	VSS	
G1	VSS	VSS	
G13	VSS	VSS	
G16	VSS	VSS	AA32
G19	VSS	VSS	AB32
G24	VSS	VSS	AD32
G28	VSS	VSS	AF28
G29	VSS	VSS	AF29
G33	VSS	VSS	AT27
G42	VSS	VSS	AV25
G45	VSS	VSS	H50
G48	VSS	VSS	
G8	VSS	VSS	
H24	VSS	VSS	
H28	VSS	VSS	
H4	VSS	VSS	
H45	VSS	VSS	
J11	VSS	VSS	
J16	VSS	VSS	
J2	VSS	VSS	
J24	VSS	VSS	
J28	VSS	VSS	
J33	VSS	VSS	
J35	VSS	VSS	
J39	VSS	VSS	
K12	VSS	VSS	
K47	VSS	VSS	
K8	VSS	VSS	
L1	VSS	VSS	
L17	VSS	VSS	
L20	VSS	VSS	
L24	VSS	VSS	
L28	VSS	VSS	
L3	VSS	VSS	
L33	VSS	VSS	
L49	VSS	VSS	
M28	VSS	VSS	
M42	VSS	VSS	
M46	VSS	VSS	
M49	VSS	VSS	
M5	VSS	VSS	
M50	VSS	VSS	
M9	VSS	VSS	
N11	VSS	VSS	
N14	VSS	VSS	
N17	VSS	VSS	
N28	VSS	VSS	
N32	VSS	VSS	
N36	VSS	VSS	
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N44	VSS	VSS	
N49	VSS	VSS	
N7	VSS	VSS	
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R49	VSS	VSS	
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T47	VSS	VSS	
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U50	VSS	VSS	
V2	VSS	VSS	
V3	VSS	VSS	

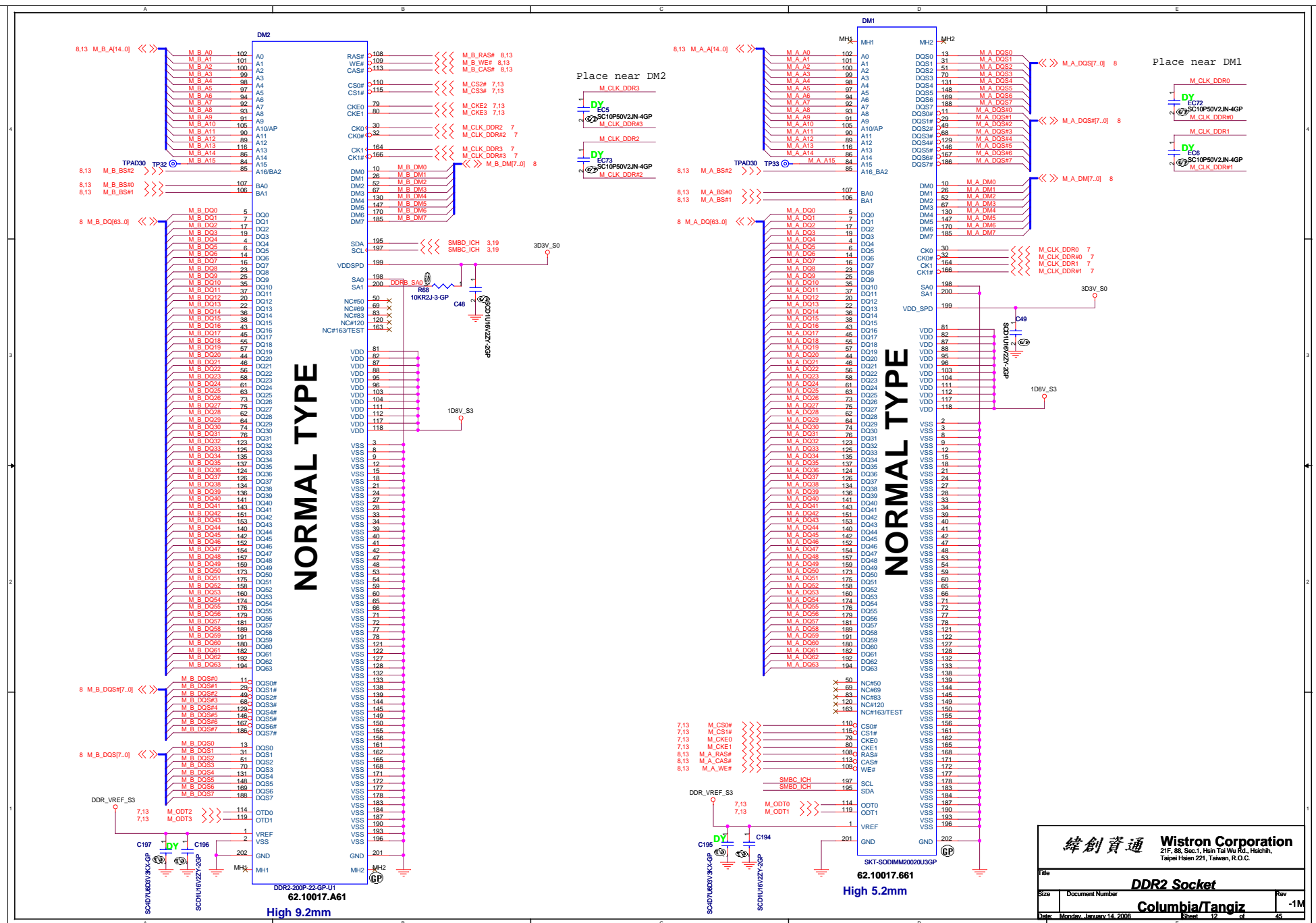
VSS

CRESTLINE-GP-U

緯創資通

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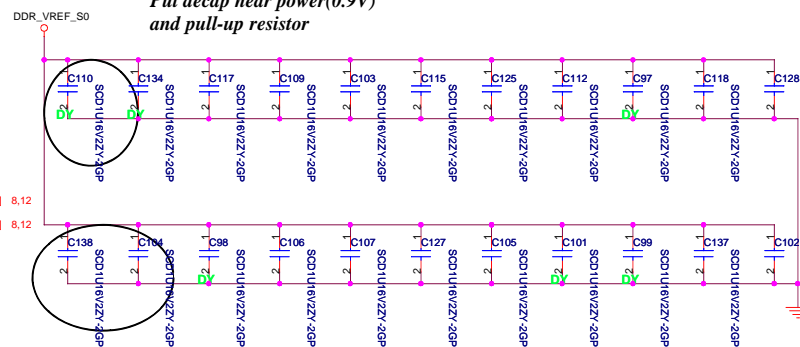
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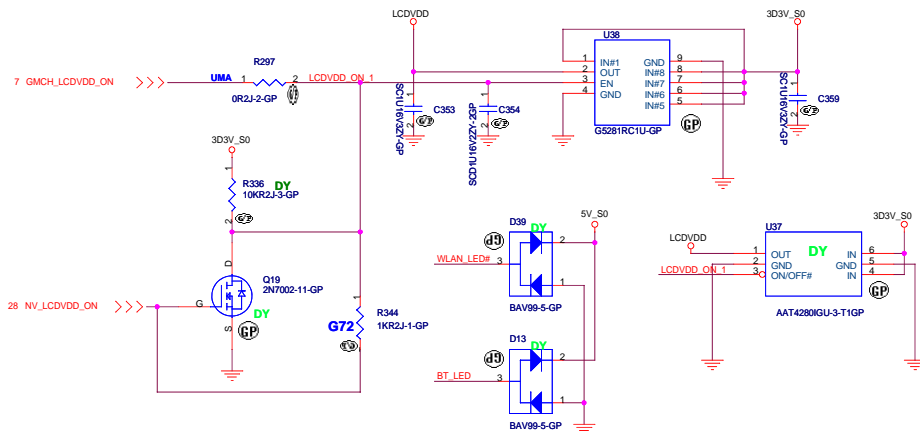


Put decap near power(0.9V) and pull-up resistor

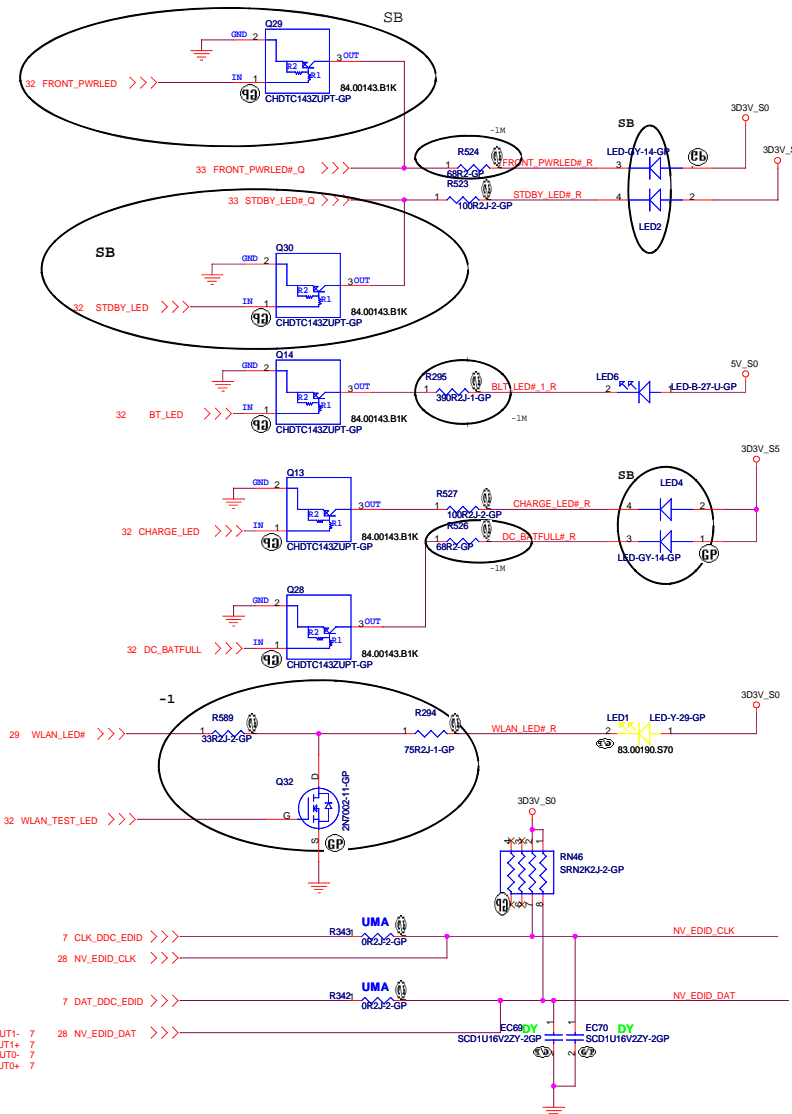
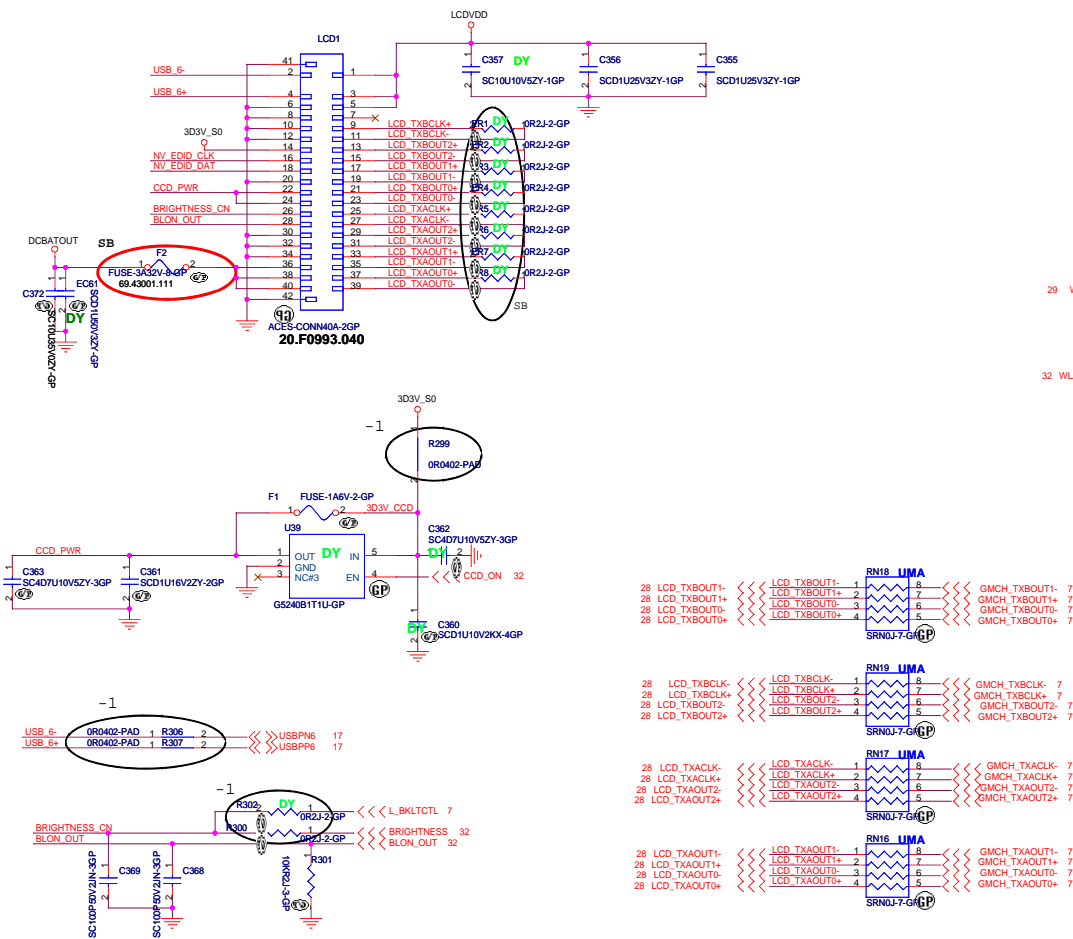


*Put decap near power(0.9V)
and pull-up resistor*





LCD/INVERTER CONN



<Variant Name>

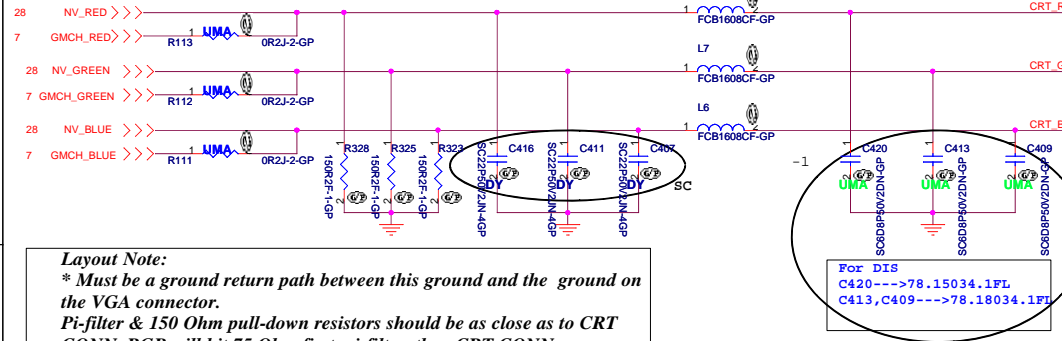
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LCD CONN & LED	Columbia/Tangiz	-1
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CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

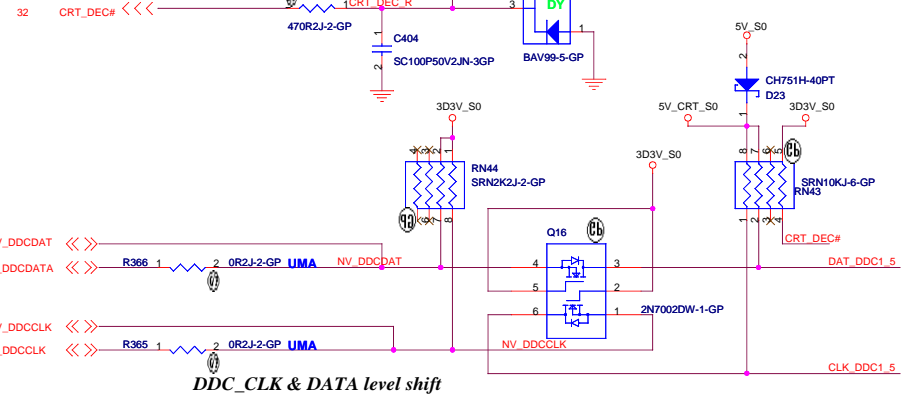
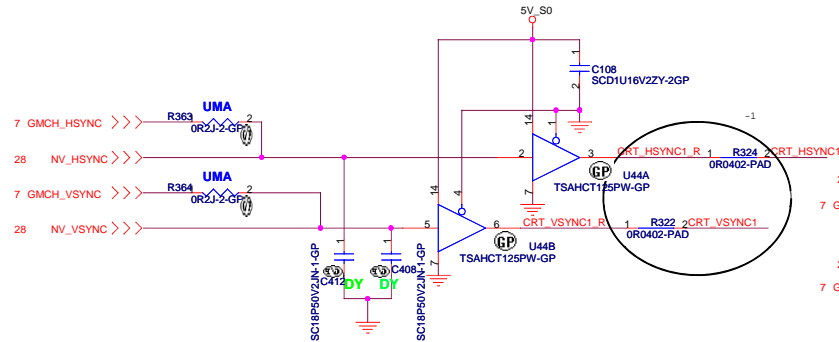
Ferrite bead impedance: 10 ohm@100MHz



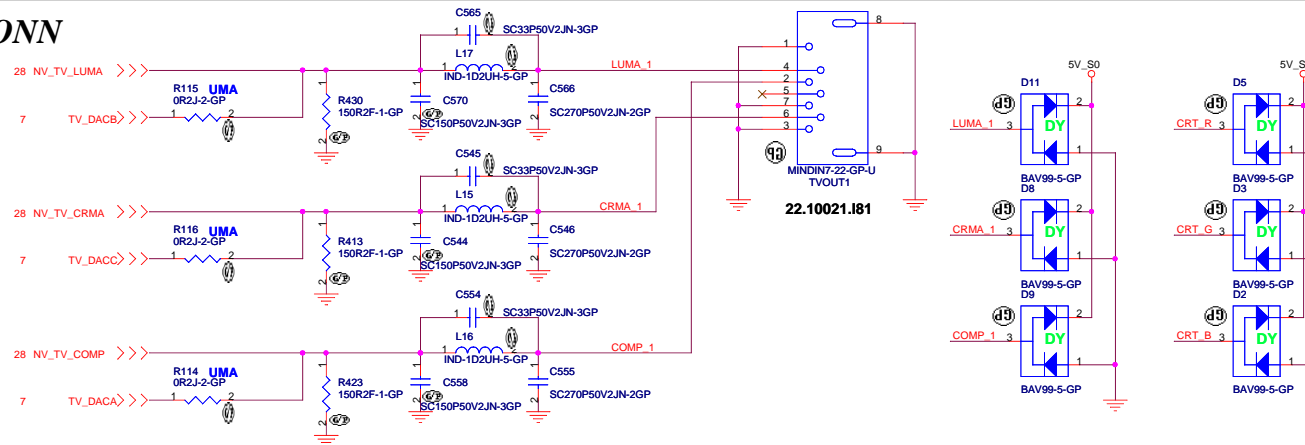
Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

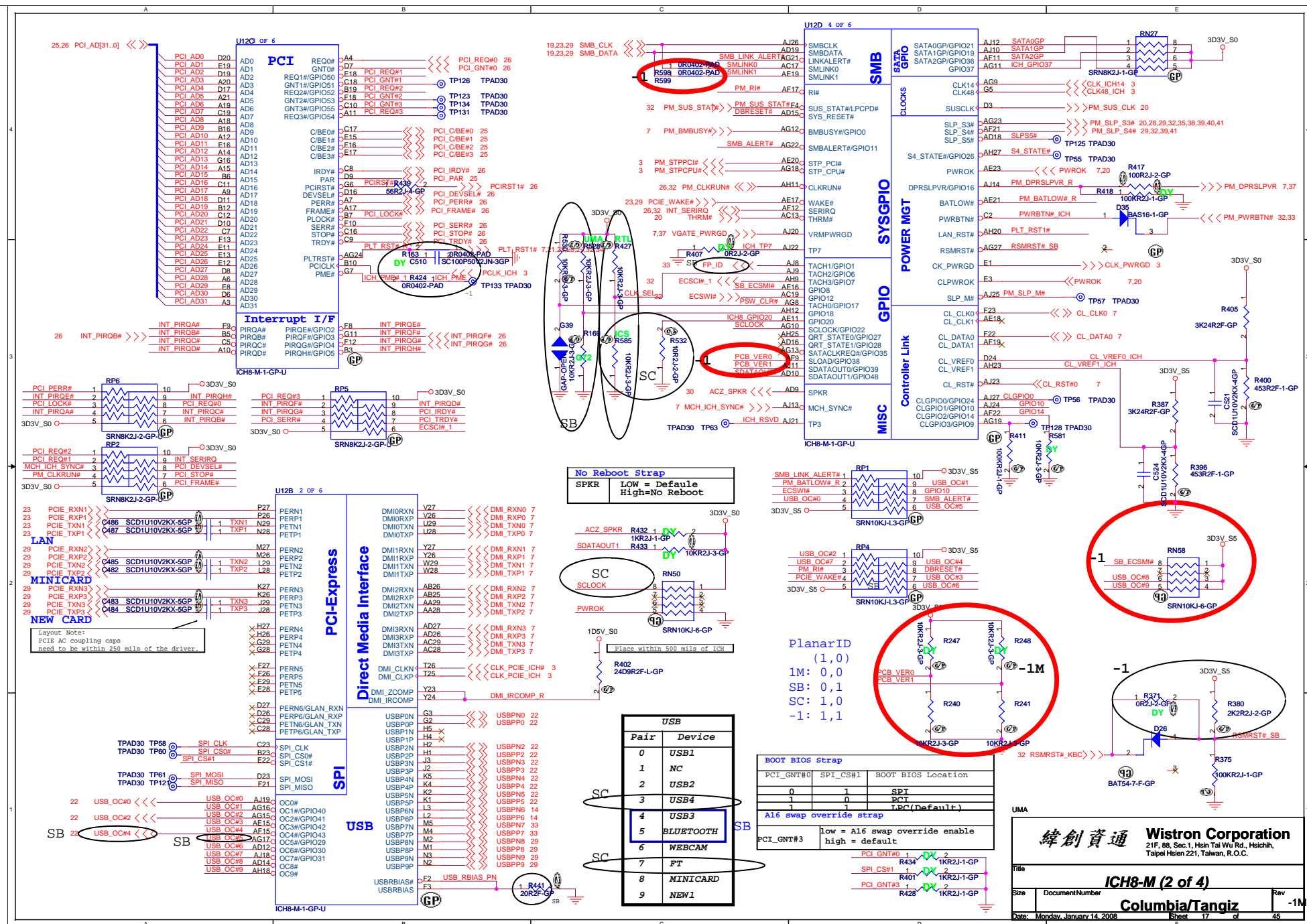


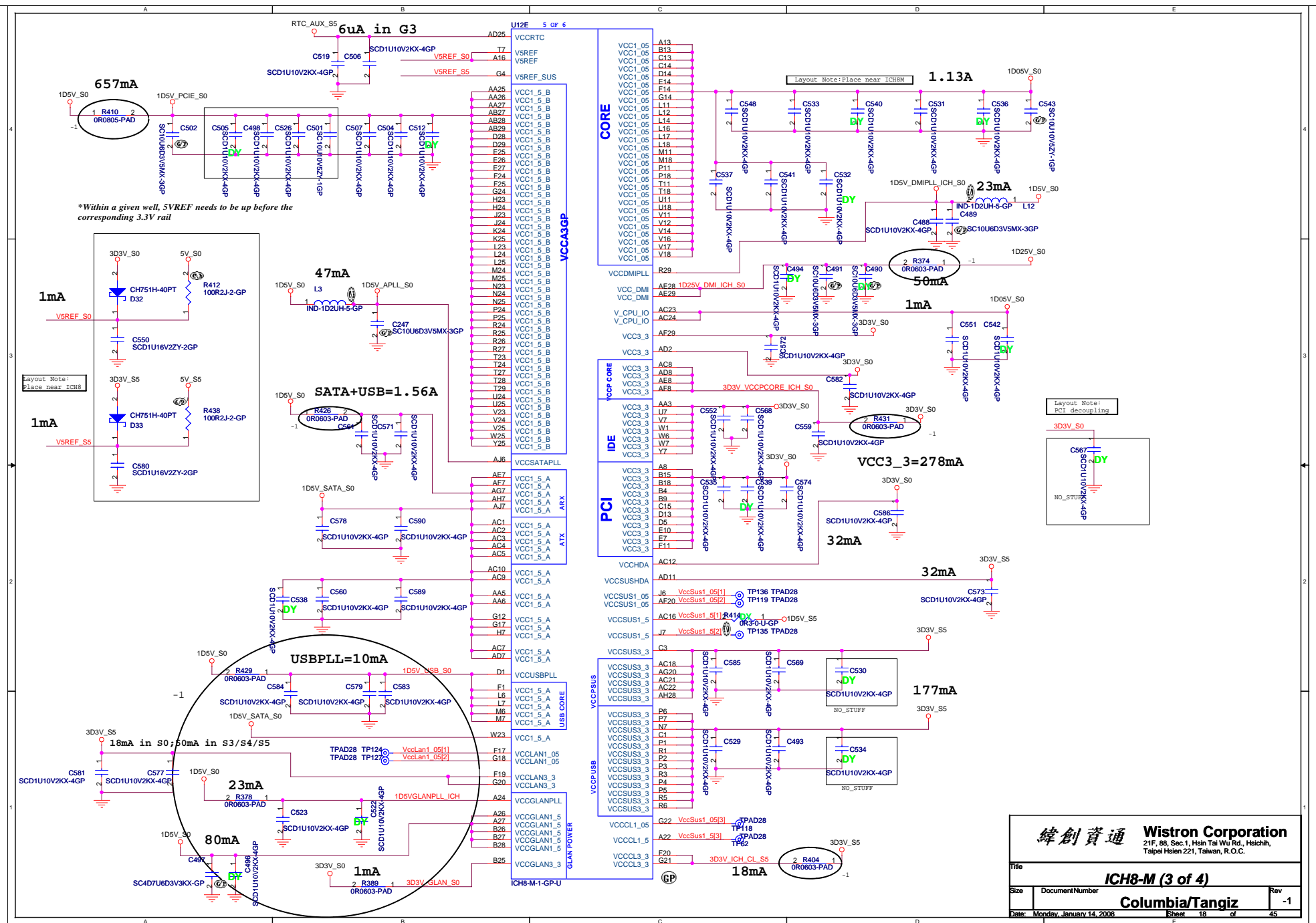
TV CONN

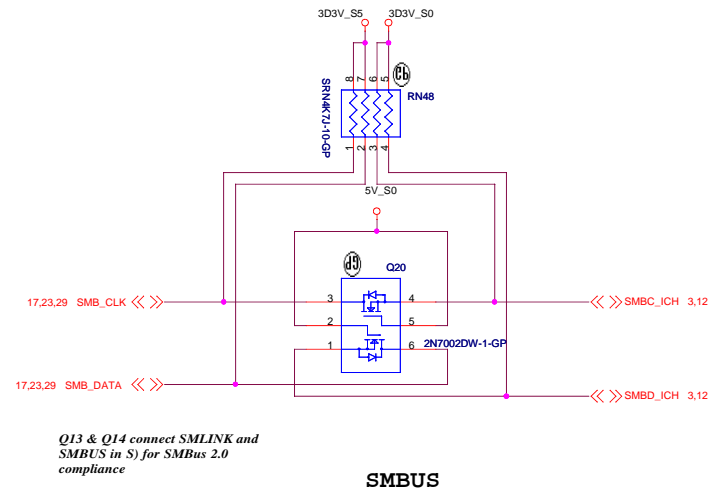


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CRT/TV Connector		
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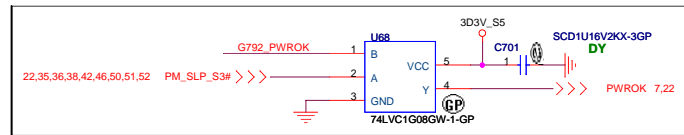




Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



-1T

Layout 15 mil

Layout 15 mil

Layout 30 mil

SB
Setting T8 as
90 Degree

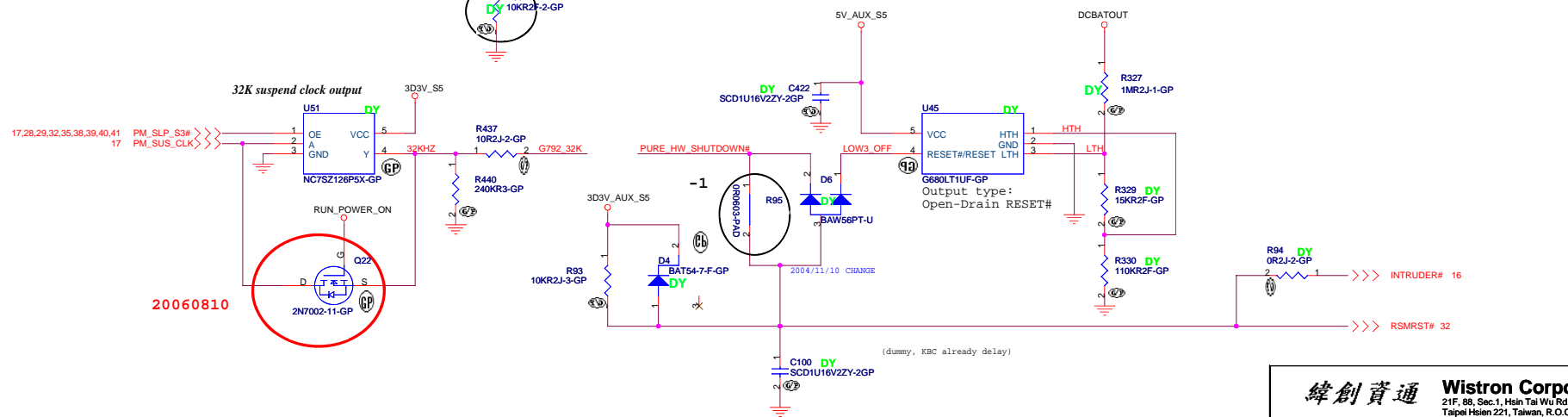
V_DEGREE
= (((Degree-72)*0.02)+0.34)*VCC

DXP1:108 Degree (CPU)
DXP2:H/W Setting 100(System)
DXP3:105 Degree (SYSTEM)

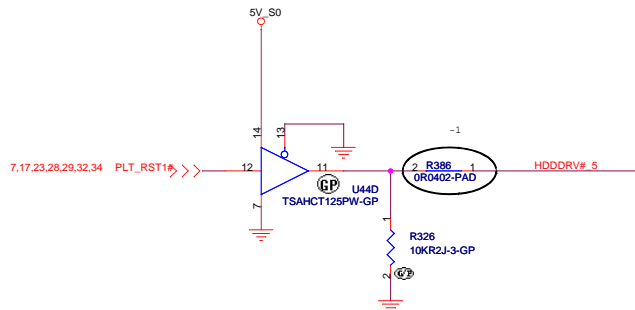
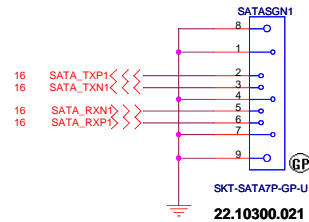
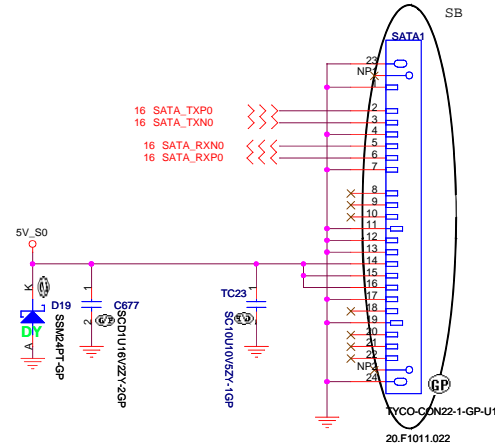
Place near chip as close
as possible

2.System Sensor,
Put between CPU and NB.

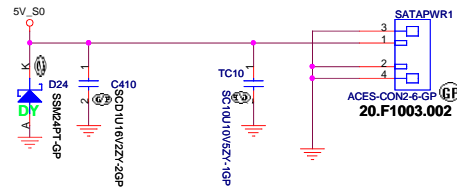
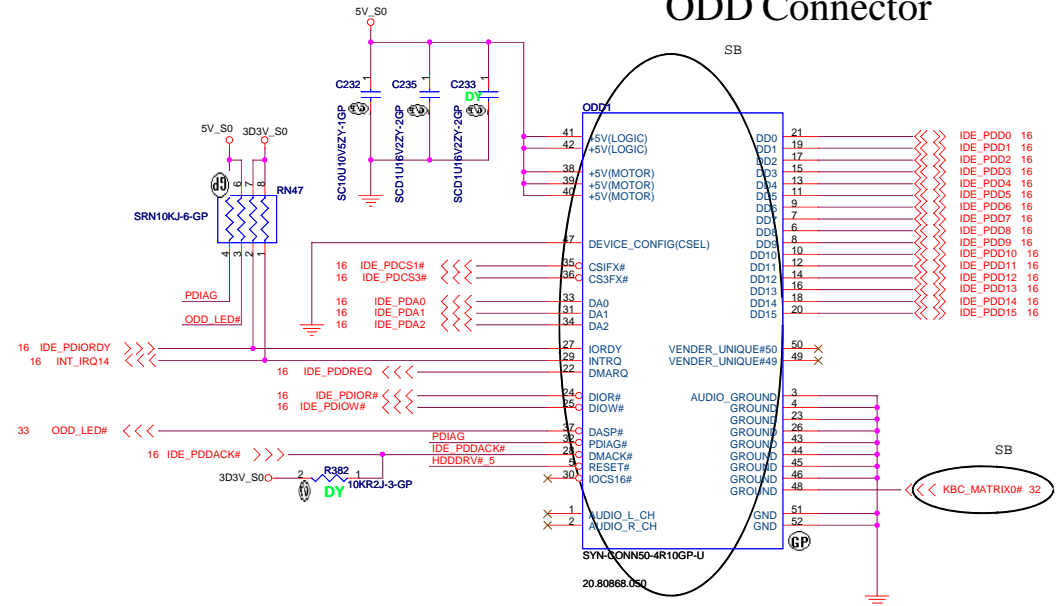
1.For CPU Sensor



SATA HD Connector

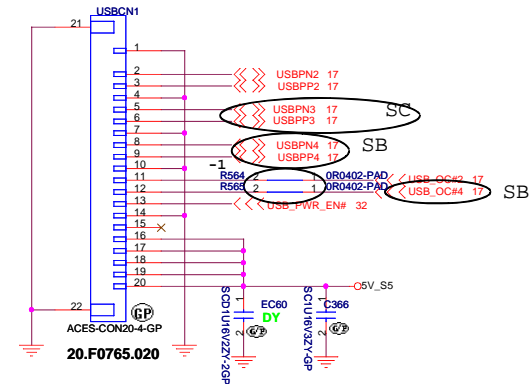
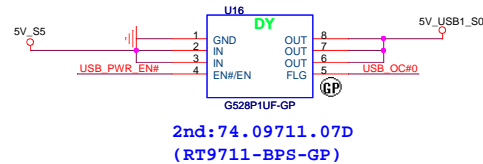
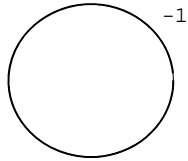
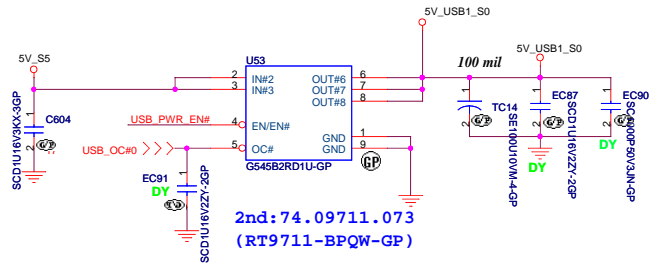


ODD Connector

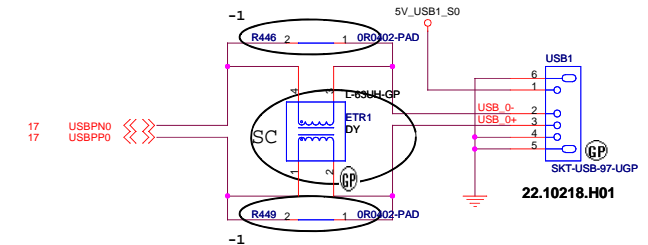
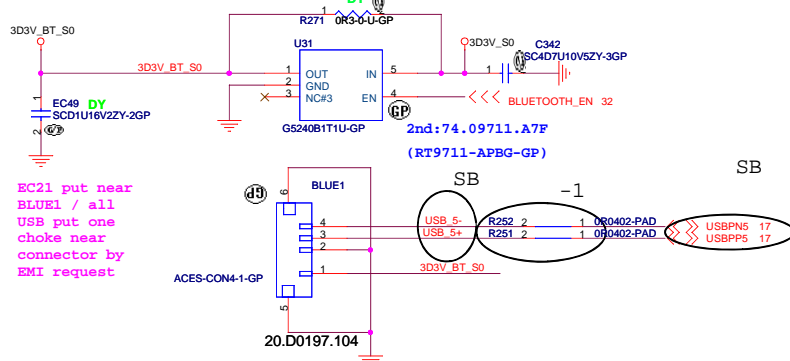


bom1

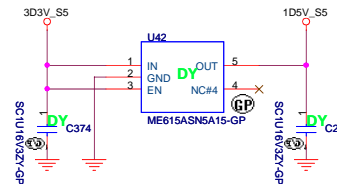
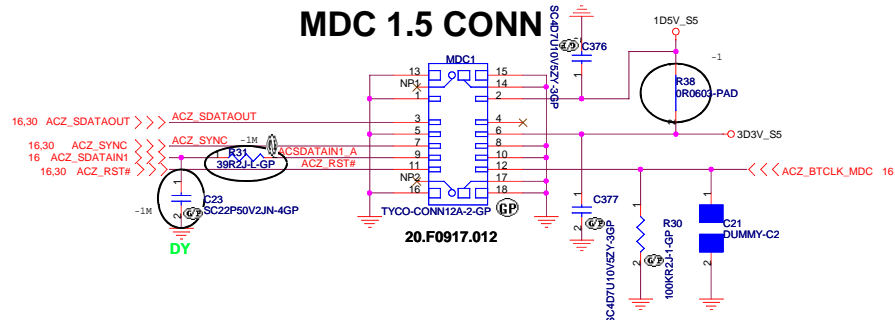
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BLUETOOTH MODULE

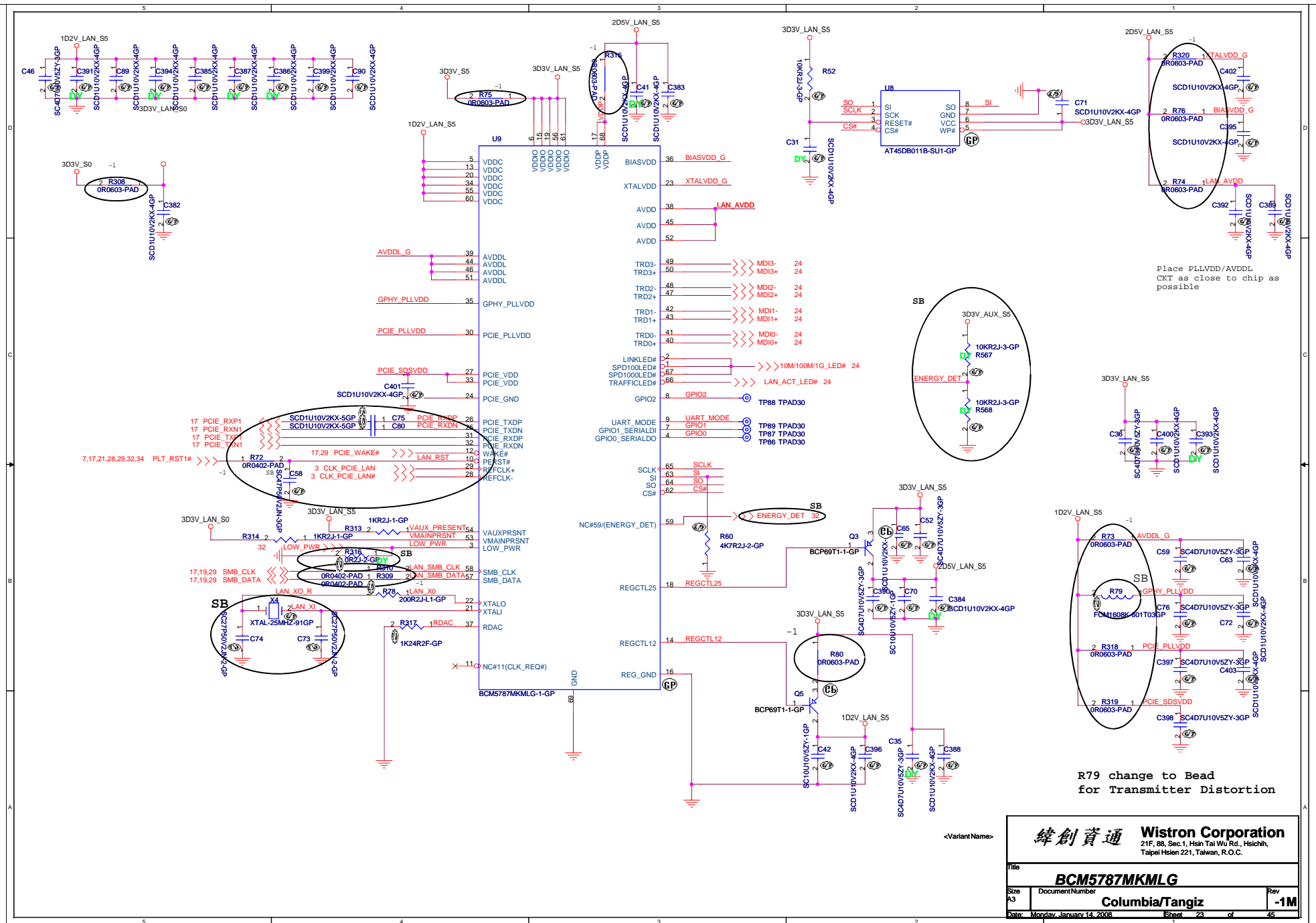


MDC 1.5 CONN

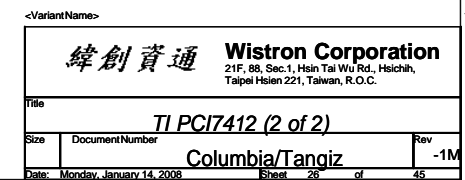


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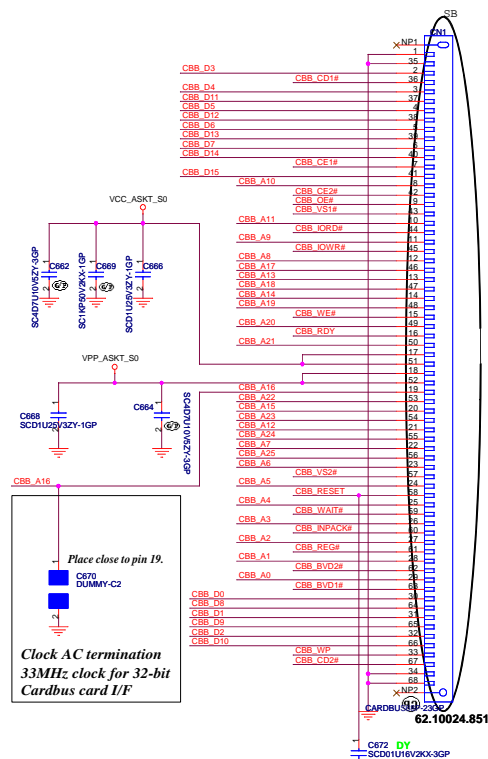
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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BCM5787MKMLG			
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Columbia/Tangiz			
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PCMCIA Socket

**Cardbus I/F**

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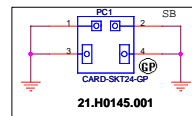
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--- <<<< CBB_WIE# 26
--- <<<< CBB_REG# 25
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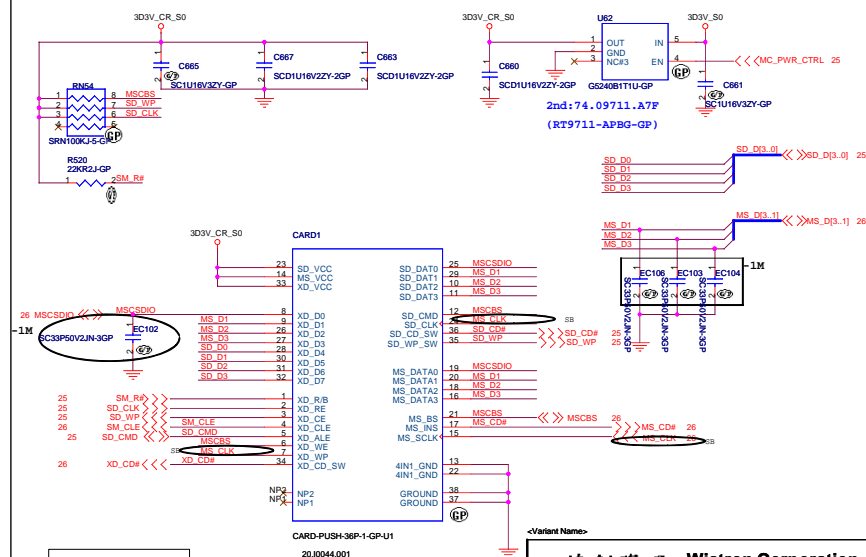
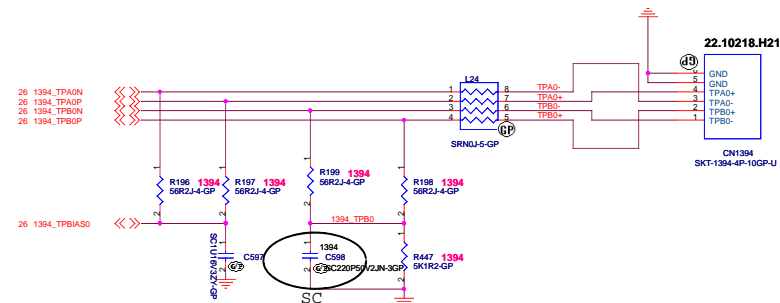
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1394 Connector



XD
MS / MS PRO
SD / SD IO / MMC

20.10044.001

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title *PCMCIA / 1394 / CARD READER*

Size	Document Number
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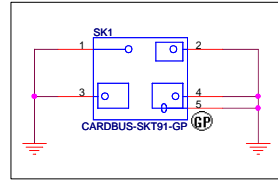
Columbia/Tangiz

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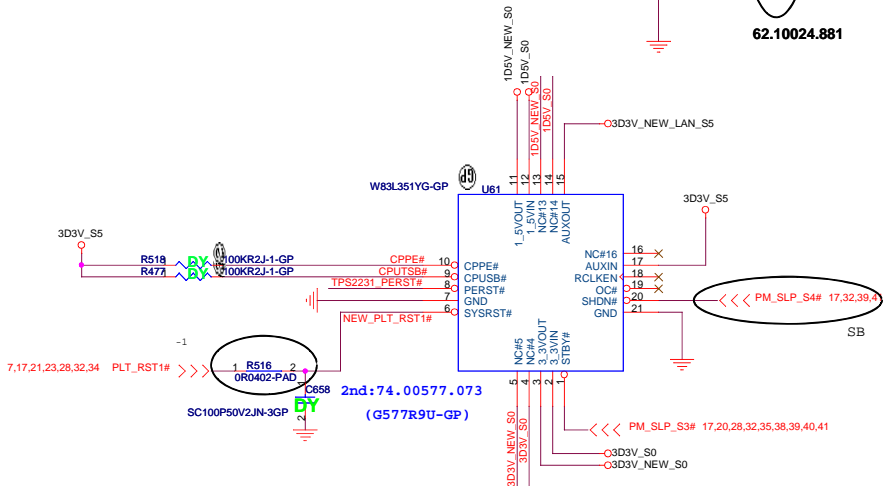
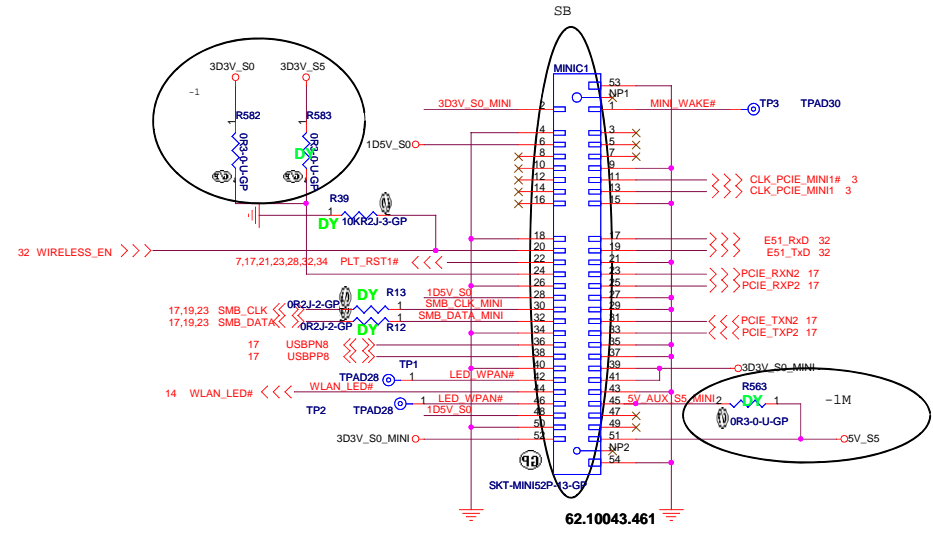
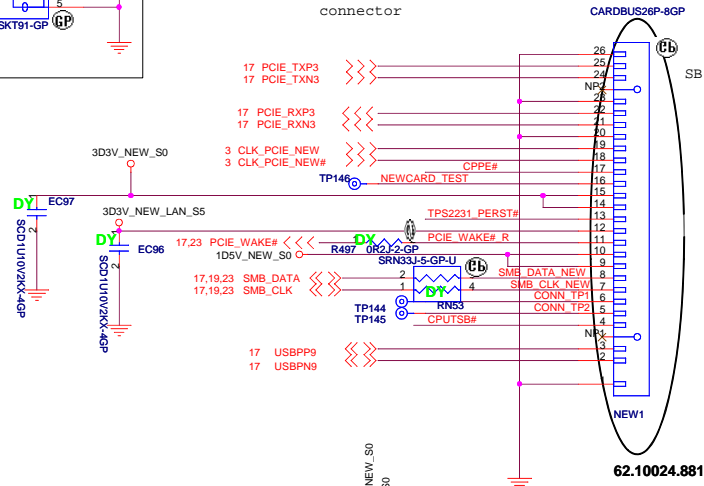
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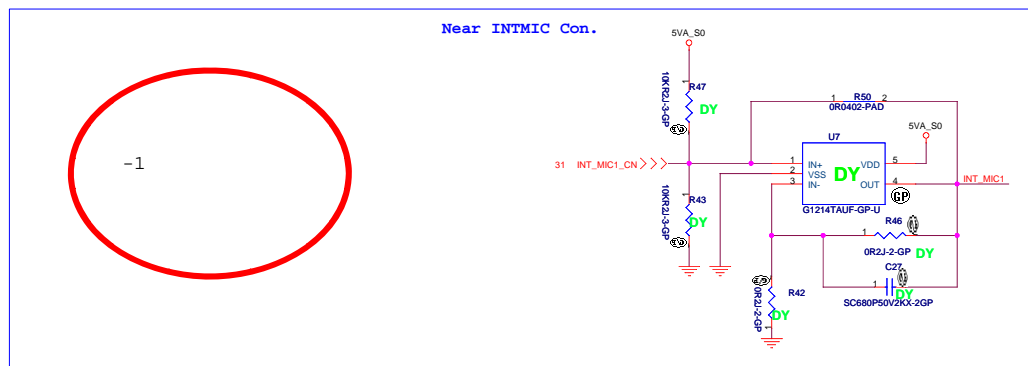
Mini Card Connector



NEWCARD Connector

Reserve the symbol
for bottom side
connector

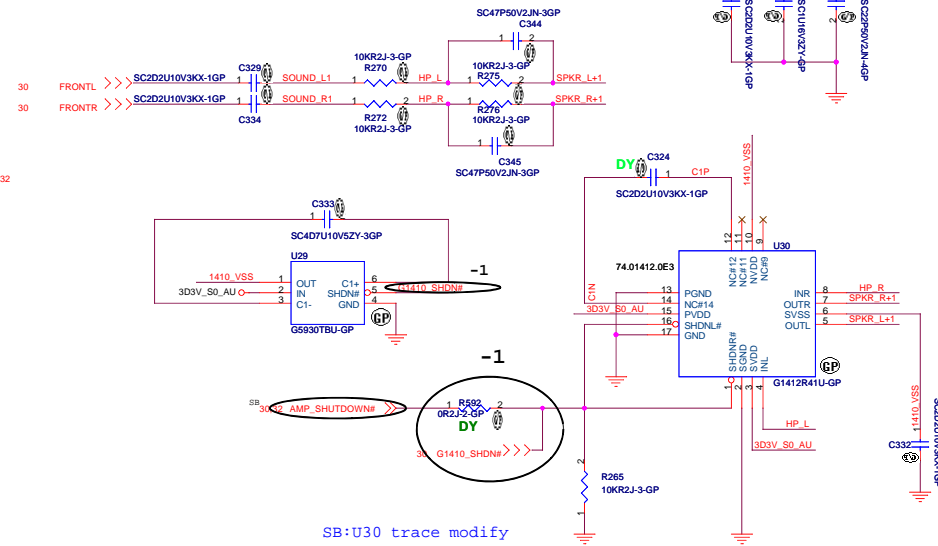
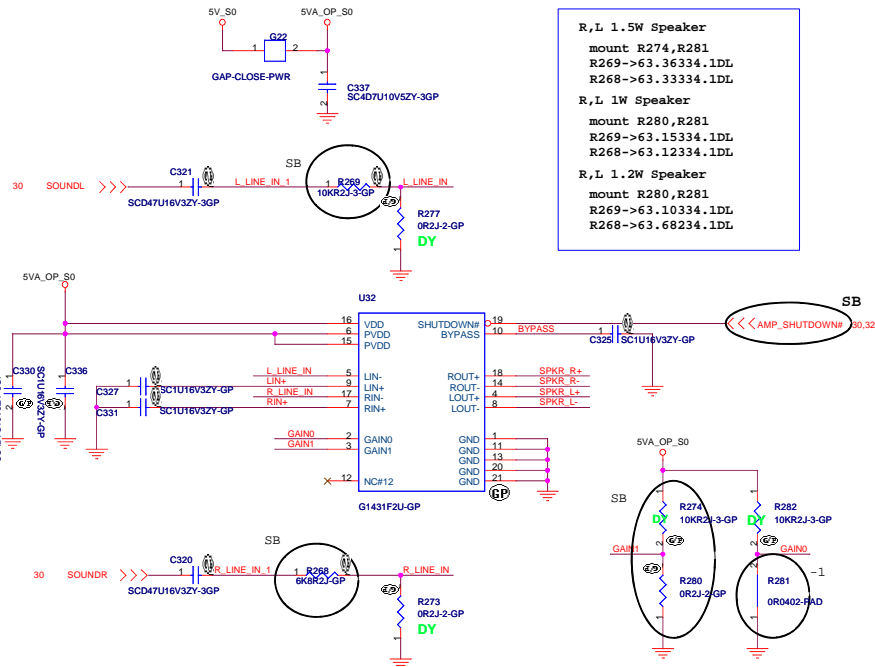




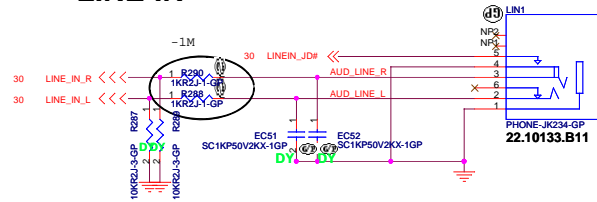
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AUDIO OP AMPLIFIER

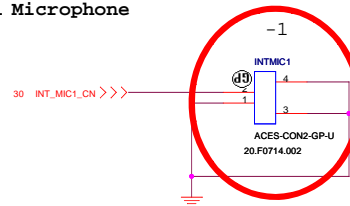
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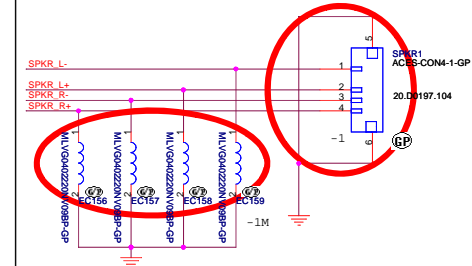
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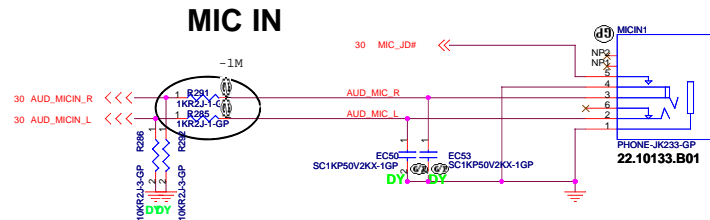
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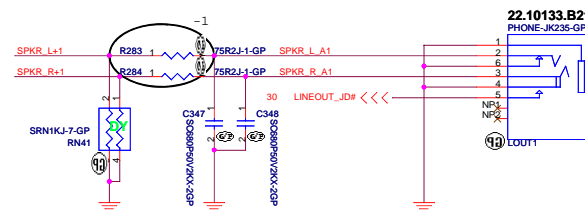
Internal Speaker



MIC IN



LINE OUT

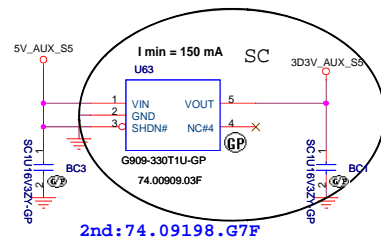


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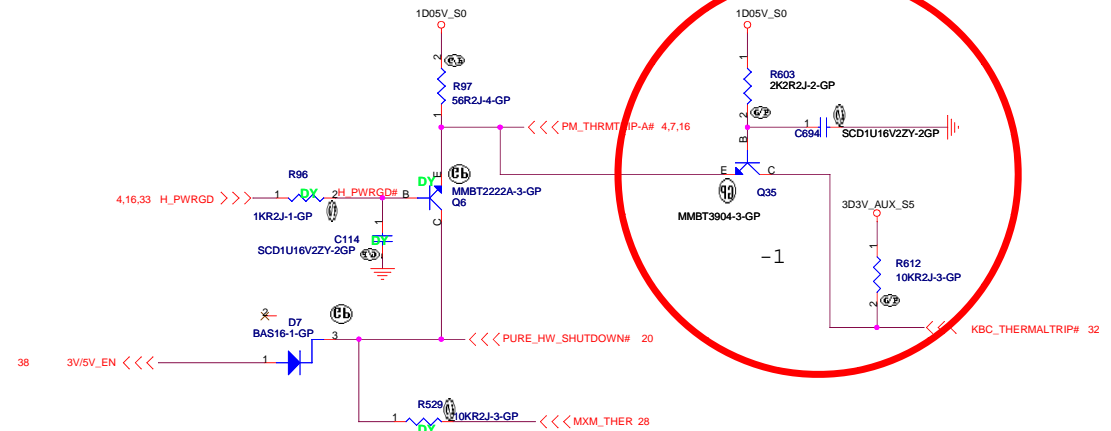
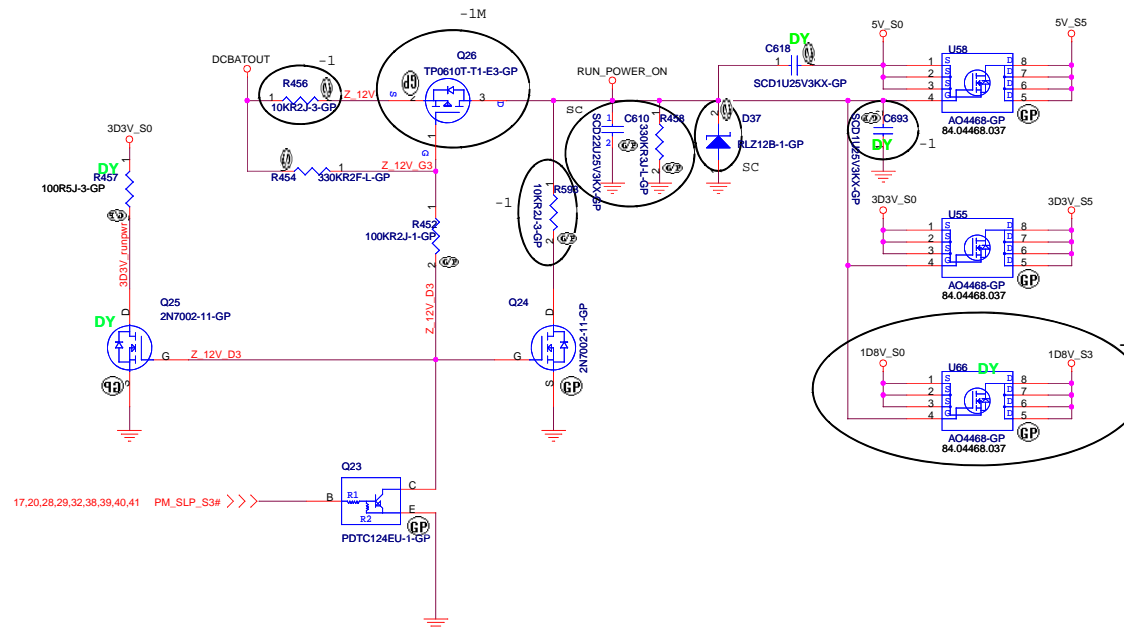
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
 Taipei Hsien 221, Taiwan, R.O.C.

File: AUDIO AMP AND JACK
 Size: Document Number
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Aux Power 3D3V_AUX_S5

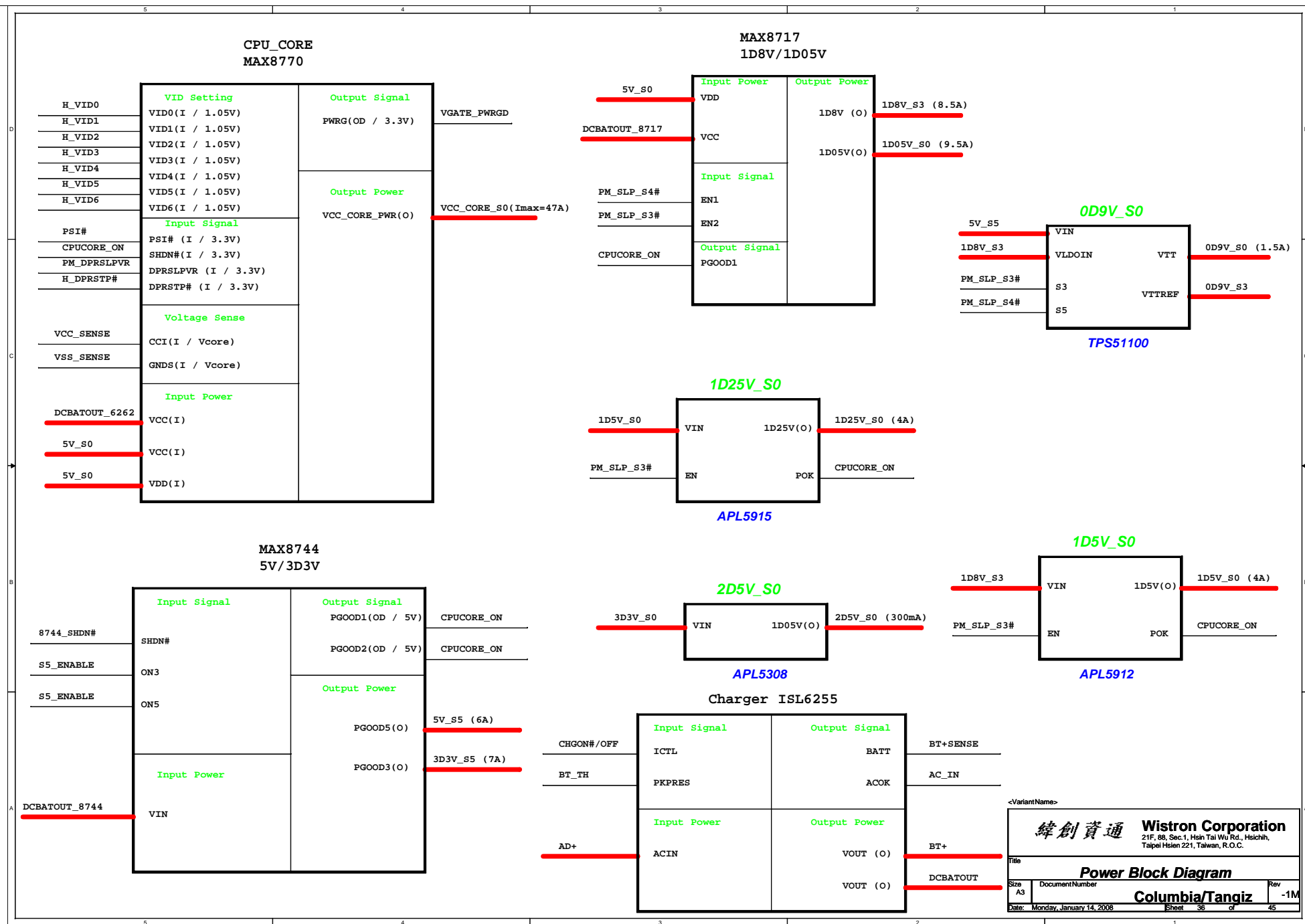


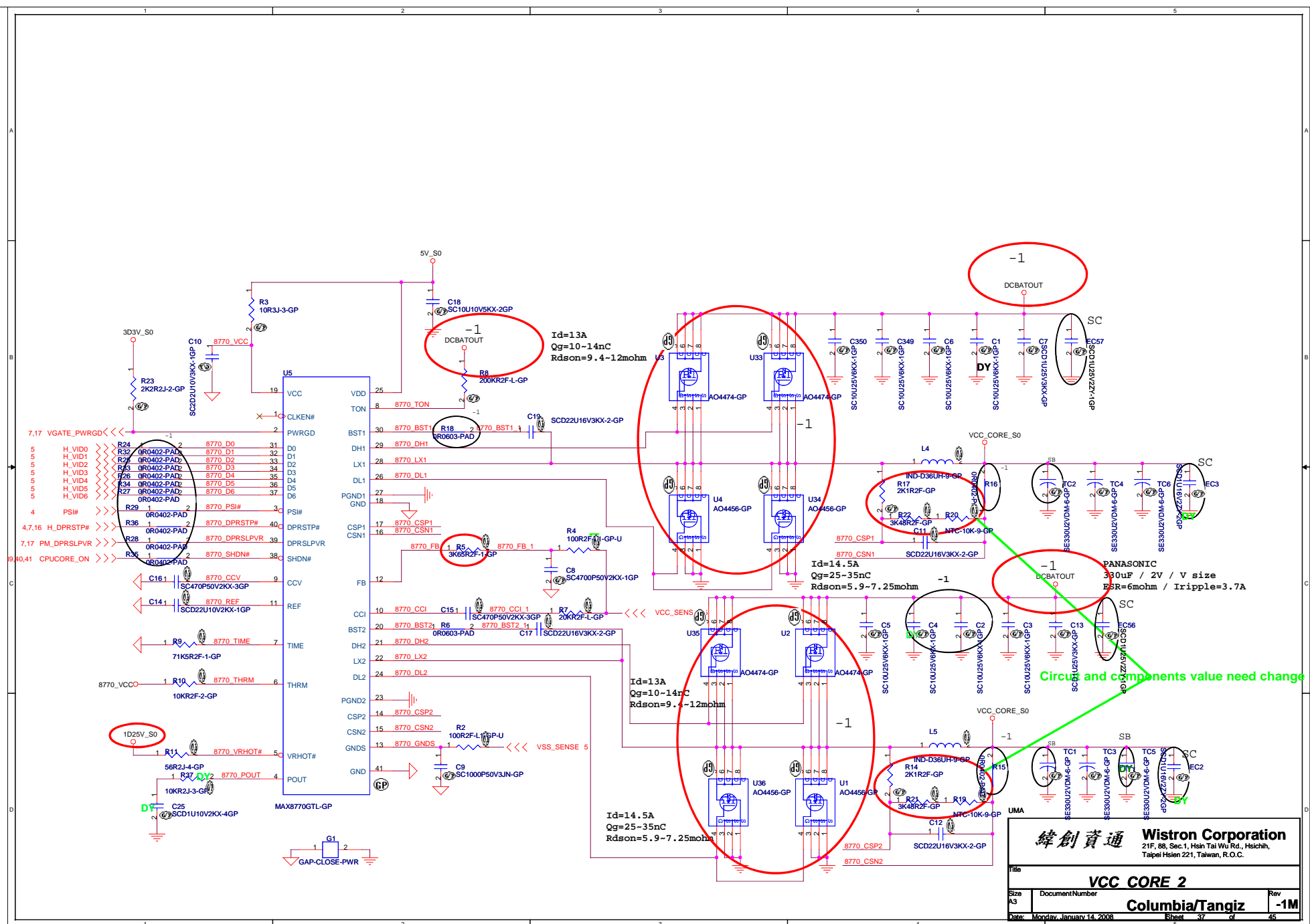
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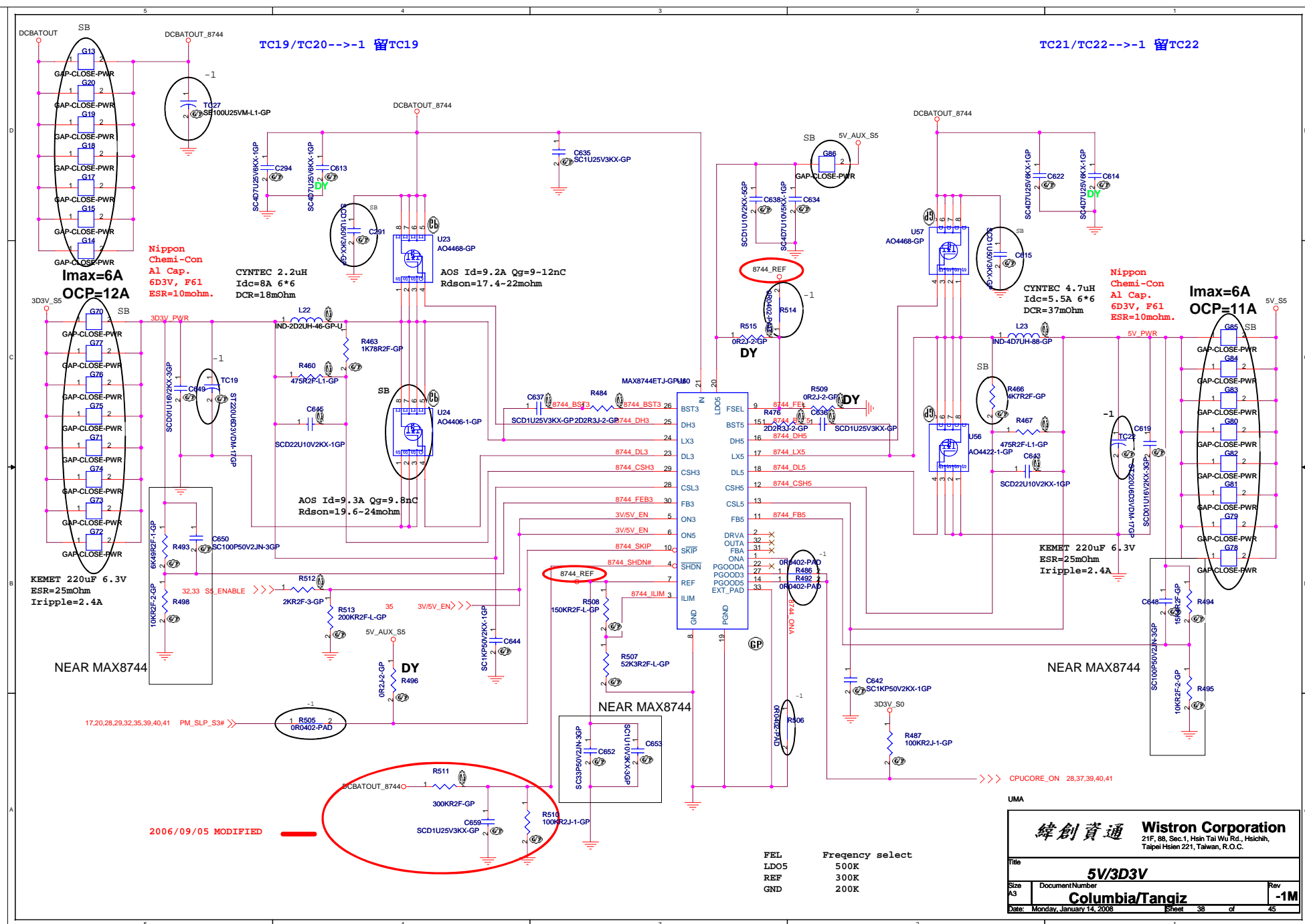


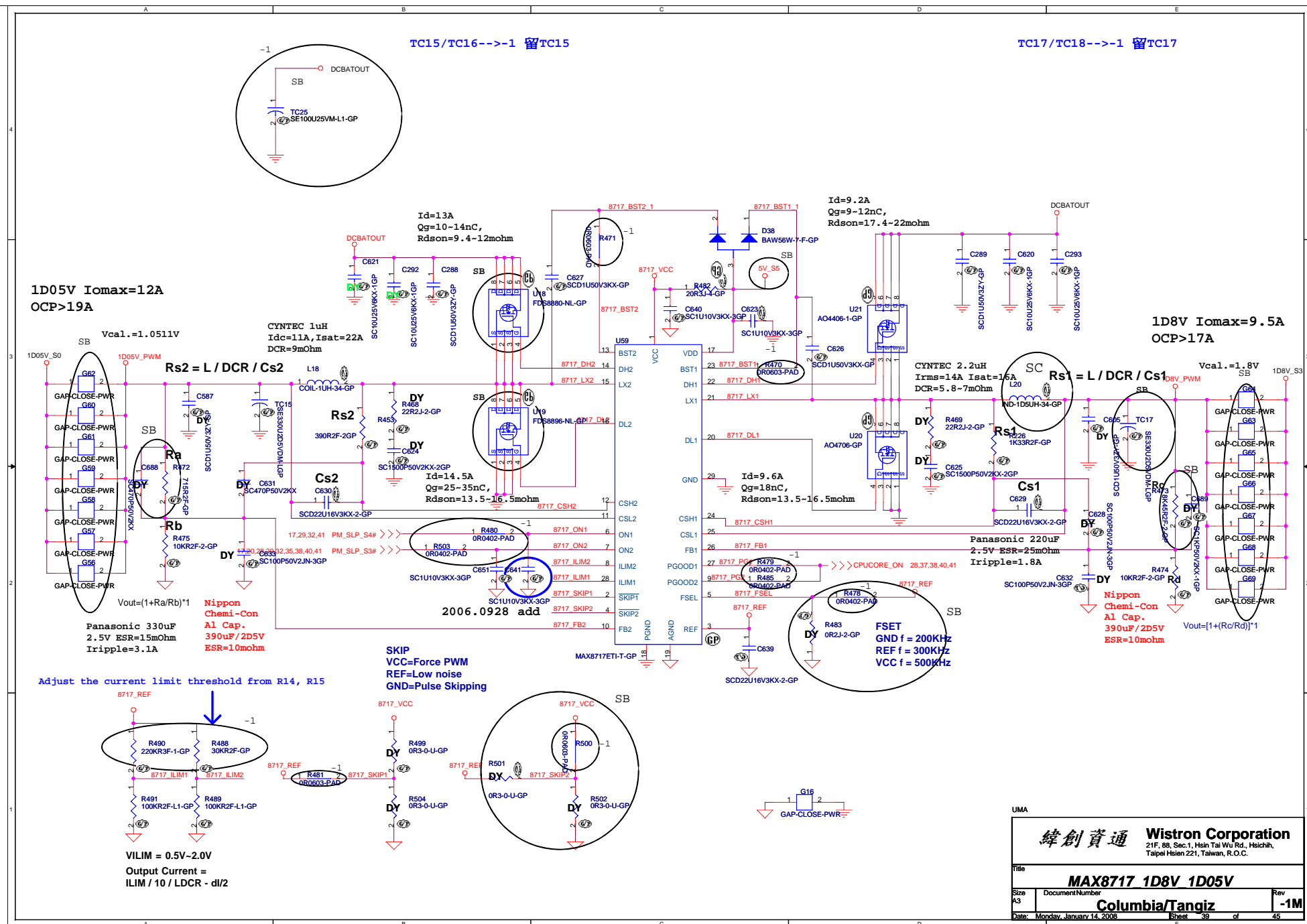
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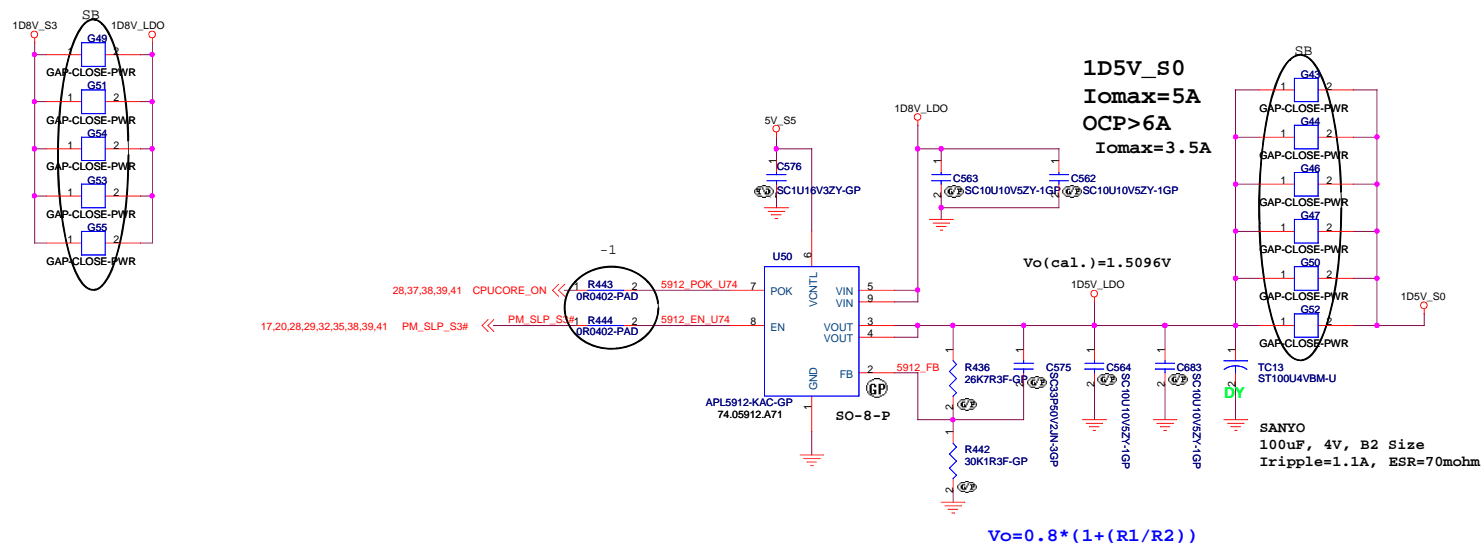
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Heiluh, Taipei Hsien 221, Taiwan, R.O.C.	
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Size	Document Number		Rev
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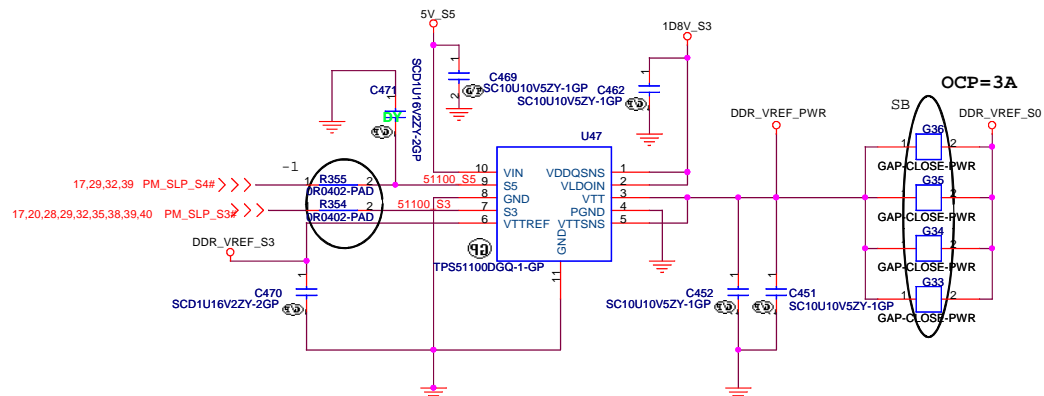


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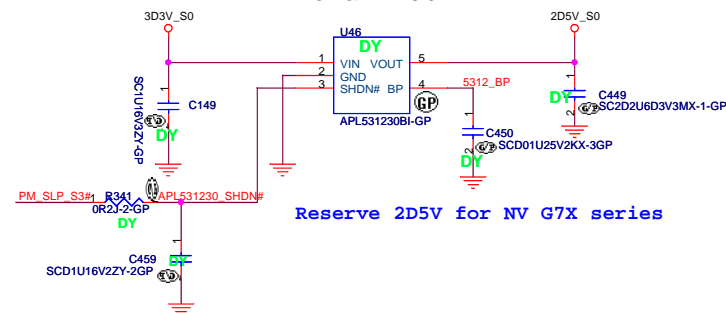
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipai Hsien 221, Taiwan, R.O.C.

Title APW5912_1D5V
Size DocumentNumber Columbia/Tangiz Rev -1M
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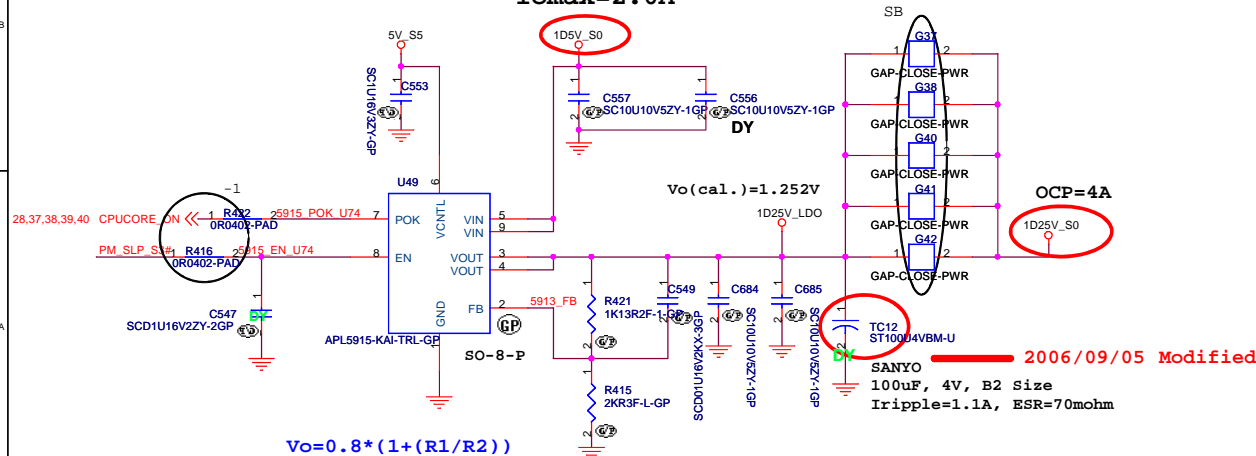
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2D5V Iomax=130mA



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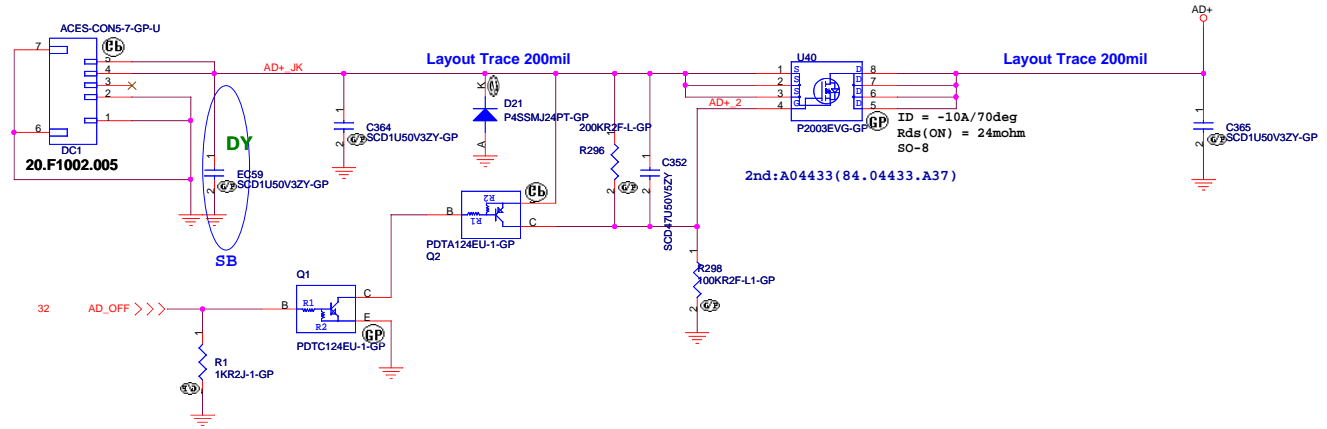


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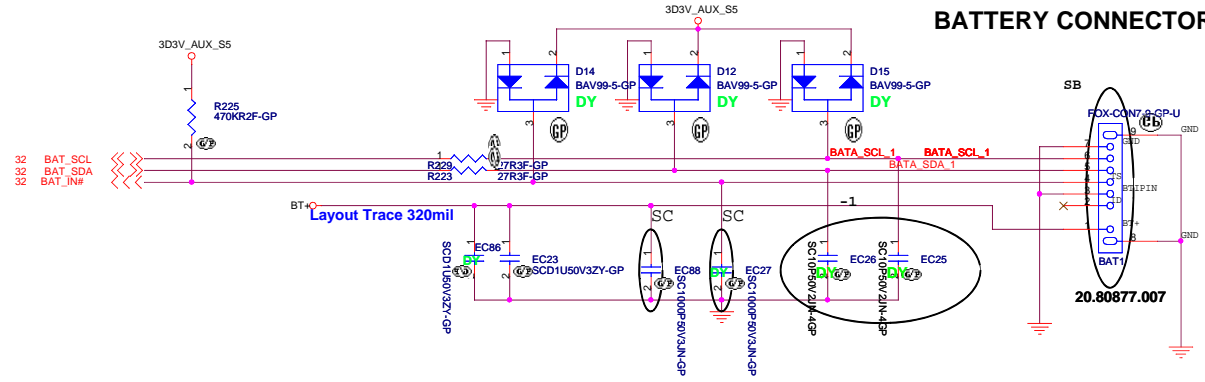
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		1D25V/2D5V//1D05V/0D9V	
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Adaptor in to generate DCBATOUT

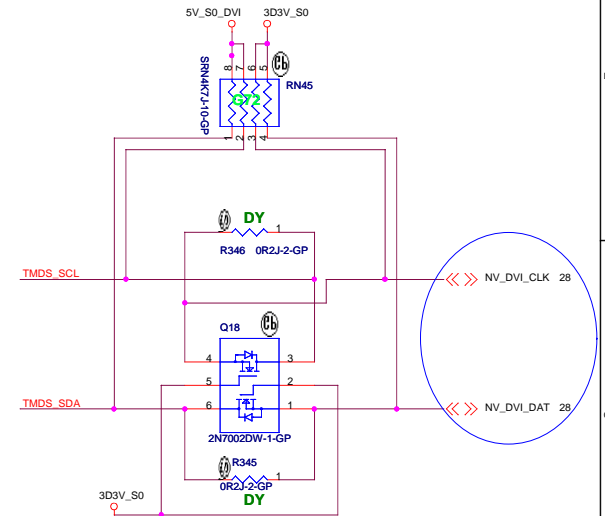
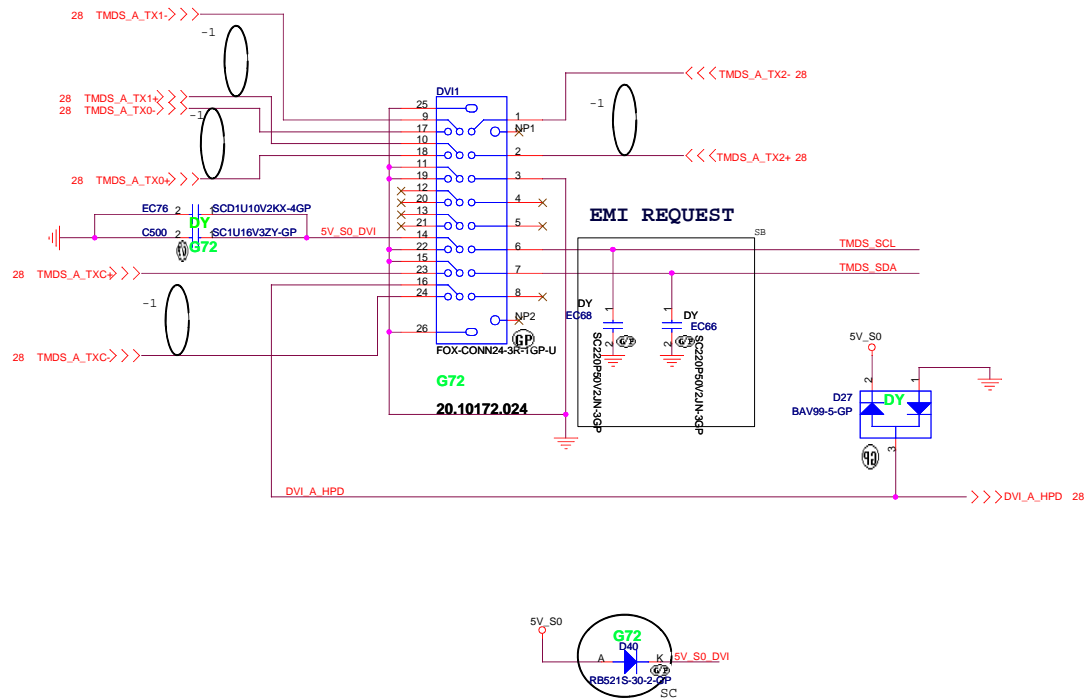


BATTERY CONNECTOR



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Title	AD/BATT CONN
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<VariantName>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
DVI CONNECTOR		Document Number	
Size A3		Rev -1M	
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